US005363000A

United States Patent [19]

Miyatake et al.

[11] Patent Number: 5,363,000

[45] Date of Patent: Nov. 8, 1994

[54] SOLID-STATE IMAGE SENSING APPARATUS

[75] Inventors: Shigehiro Miyatake, Osaka; Kenji Takada, Itami; Kouichi Ishida, Amagasaki; Kouichi Sameshima, Itami, all of Japan

[73] Assignee: Minolta Co., Ltd., Osaka, Japan

[21] Appl. No.: 12,575

[22] Filed: Feb. 3, 1993

[30] Foreign Application Priority Data

Feb. 5, 1992 [JP] Japan 4-019337

[51] Int. Cl.[5] H03K 5/01; G06F 7/556

[52] U.S. Cl. 327/350; 327/514; 327/515

[58] Field of Search 307/311, 315, 492, 228, 307/263, 246; 330/257; 323/314, 315, 316, 317; 328/127, 181, 145, 185

[56] References Cited

U.S. PATENT DOCUMENTS

3,240,944	3/1966	Wolfson et al.	307/311
4,085,411	4/1978	Genesi .	
4,241,262	12/1980	Audaire et al.	307/228
4,384,300	5/1983	Iizuka	307/291
4,447,746	5/1984	Fang	307/311
4,467,191	8/1984	Chalfin et al.	307/311
4,473,836	9/1984	Chamberlain	357/30
4,536,702	8/1985	Nagano	323/314
4,584,606	4/1986	Nagasaki	358/209
4,598,414	7/1986	Dries	377/58
4,617,481	10/1986	Masuda	328/127
4,742,238	5/1988	Sato	250/578
4,742,380	5/1988	Chang	357/23.4
4,745,446	5/1988	Cheng	357/22
4,769,619	9/1988	Taylor	323/316
4,791,396	12/1988	Nishizawa	357/22
4,841,349	6/1989	Nakano	307/311
4,845,355	7/1989	Nakagawa	250/211
4,857,725	8/1989	Goodnough	307/311
4,897,614	1/1990	Nishio	330/257
4,901,129	2/1990	Hynecek	357/30
4,973,833	11/1990	Takada	250/208.1
4,990,981	2/1991	Tanaka	357/23.7
5,034,625	7/1991	Min	307/296.2
5,136,184	8/1992	Deevy	307/362

FOREIGN PATENT DOCUMENTS

253960 1/1989 Japan .

Primary Examiner—Timothy P. Callahan
Assistant Examiner—Shawn Riley
Attorney, Agent, or Firm—Price, Gess & Ubell

[57] ABSTRACT

In an image sensing device, a photodiode is connected to a drain of a MOS transistor. The drain is connected to a gate of the MOS transistor via a resistor. The MOS transistor operates in a subthreshold region to output a signal being logarithmically proportional to the intensity of incident light to the photodiode.

8 Claims, 6 Drawing Sheets

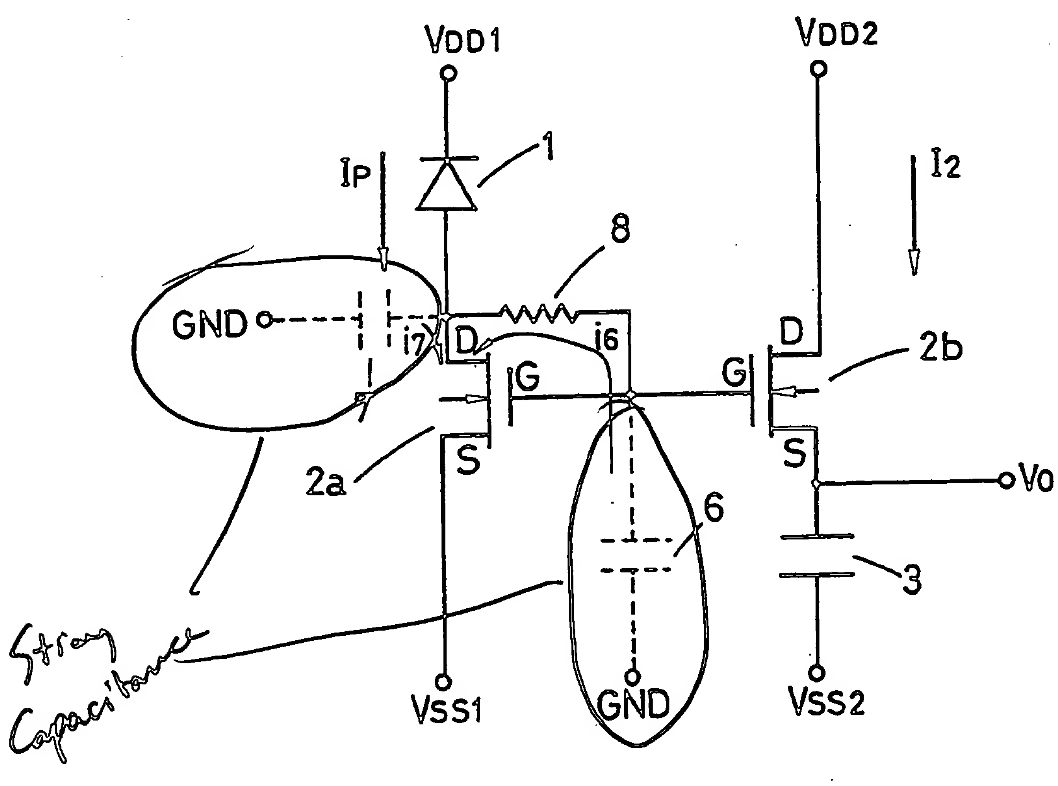


Fig. 1

Prior Art

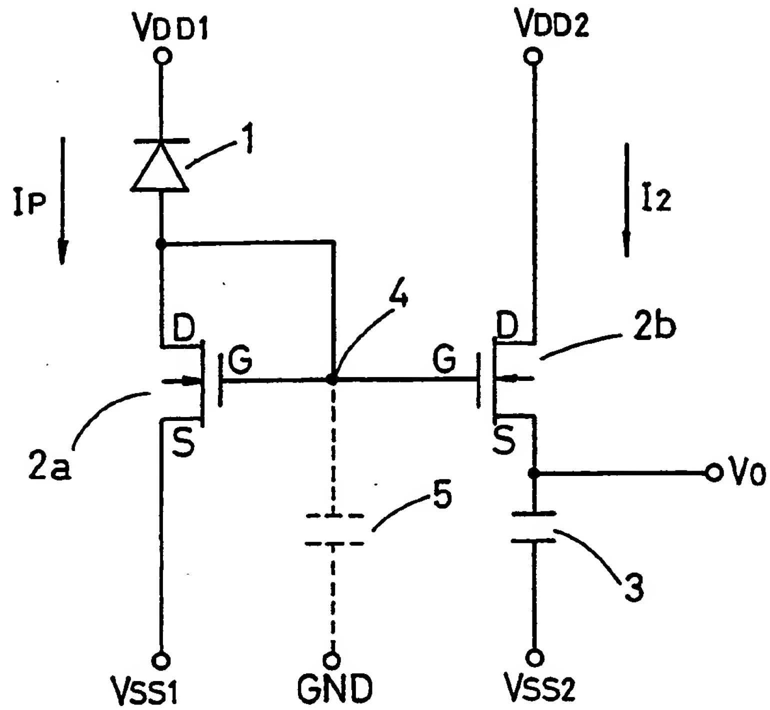


Fig. 2

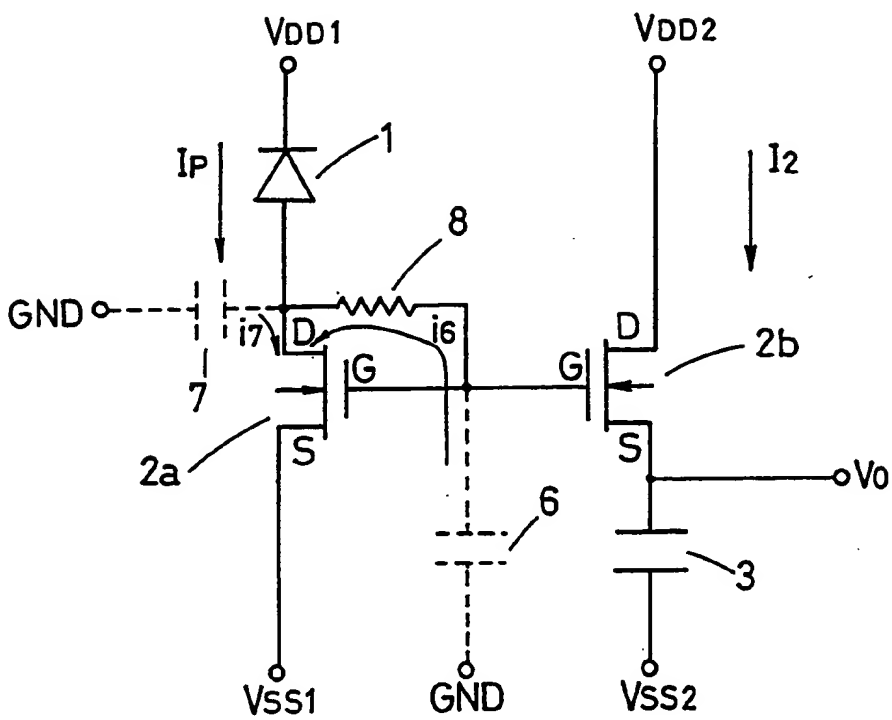


Fig. 3

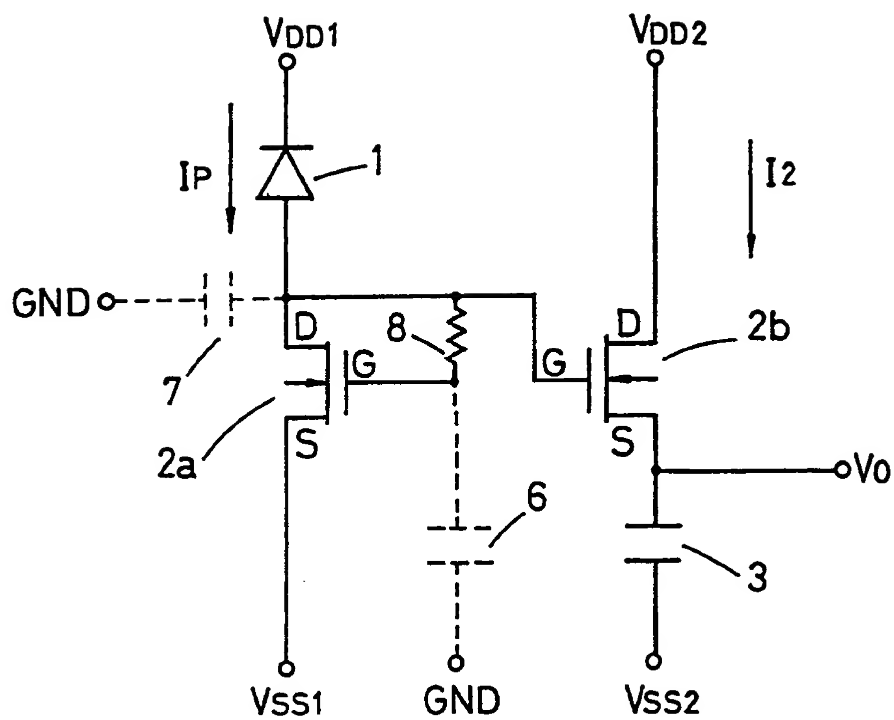


Fig. 4

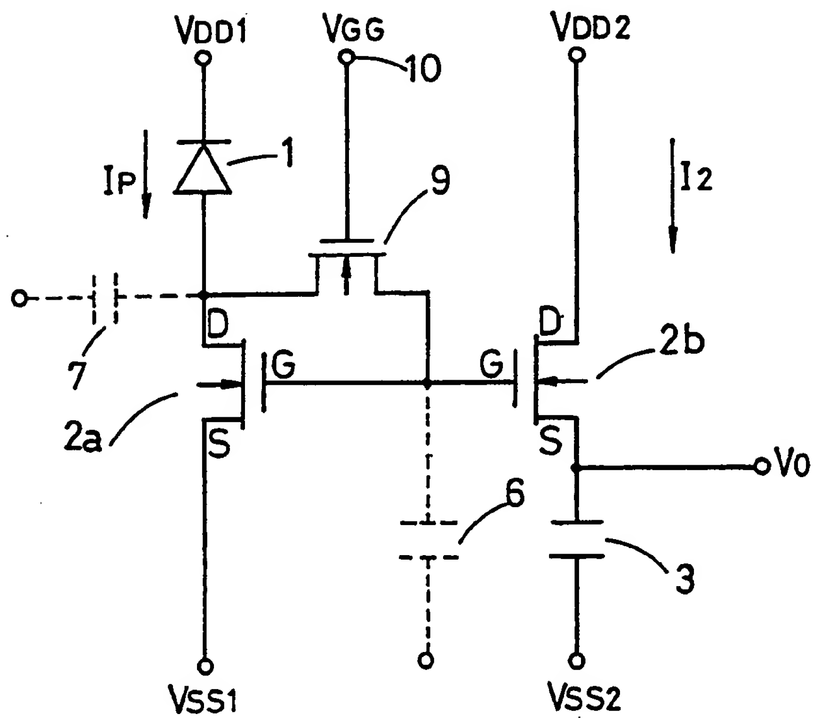


Fig. 5

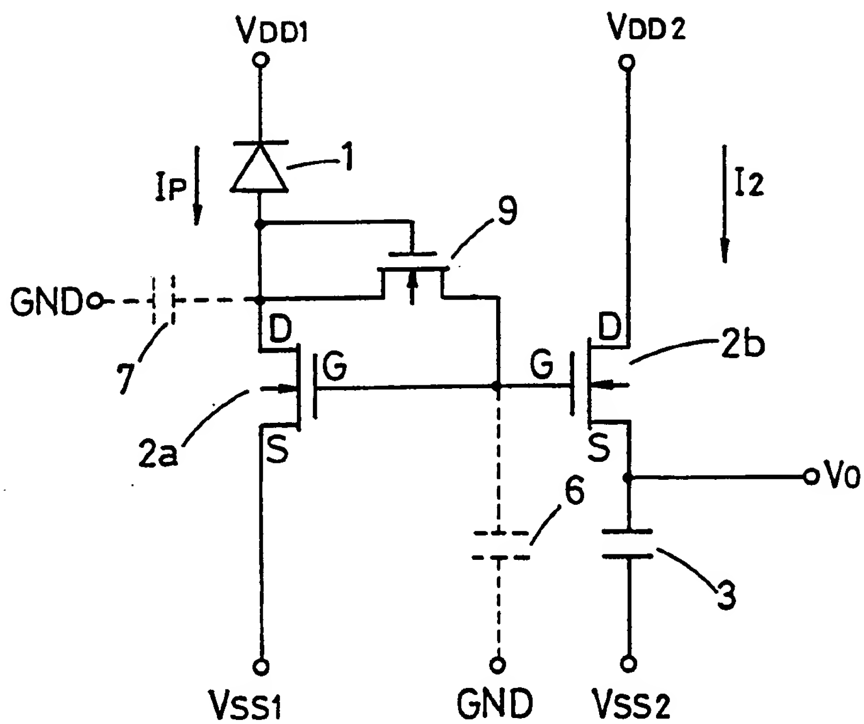
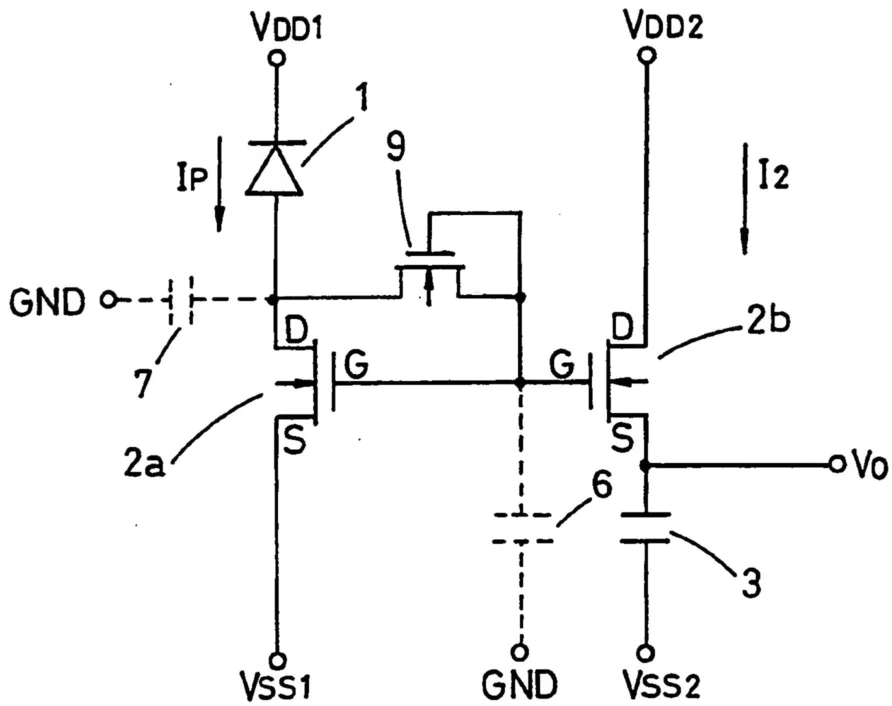


Fig. 6



SOLID-STATE IMAGE SENSING APPARATUS

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a solid-state image sensing apparatus for converting a light signal into an electric signal, and more particularly, to a solid-state image sensing apparatus where the dynamic range is expanded by the incorporation of a logarithmic conversion function. p 2. Description of the Prior Art

Solid-state image sensing apparatuses not only are smallsized, light-weight and consume less power but they also are free from image distortion and sticking and have a tolerance for environmental conditions such as vibration and magnetic fields. Since they can be manufactured by a process common or similar to that of large scale integrated circuits (LSIs), they have a high reliability and are suitable for mass production. Because of these advantages, solid-state image sensing apparatuses are widely used. For example, a linear image sensing apparatus is used in a facsimile apparatus and a two-dimensional image sensing apparatus is used in a video camera.

However, most solid-state image sensing apparatuses have defects that a precise control of the exposure amount is required since the dynamic range is small compared to that of the silver film and that even if the exposure amount is precisely controlled, a dark portion of an image is sensed as a black portion, or a bright portion is sensed as a white portion, since the dynamic range is small. As a solution to these problems, a solid-state image sensing apparatus has been proposed having a wide dynamic range and capable of sensing light of from high luminance to low luminance. The solid-state image sensing apparatus is provided with a photosensitive means capable of generating a photoelectric current which is in accordance with the intensity of incident light, a metal oxide semiconductor (MOS) transistor to which the photoelectric current is inputted and a bias means for biasing the MOS transistor so that the bias voltage thereof is equal to or below a threshold voltage and that the subthreshold current can flow therethrough. A characteristic region where the subthreshold current flows is hereinafter referred to as a subthreshold region. The logarithmic compression conversion of the photoelectric current is made by using the MOS transistor in a subthreshold region.

FIG. 1 shows an arrangement of a circuit corresponding to one pixel of a solid-state image sensing apparatus of Japanese Patent Application H1-334472 of the present applicant.

In this circuit, when $V_O = V_{OI}$ at t=0, if the substrate bias effect is ignored, the following equation (1) is obtained:

$$V_0 = V_{SS1} + \frac{nkT}{q} \ln\left[\frac{q}{nkTC}\int I_P dt + \exp\left(\frac{q}{nkT}(V_{0I} - V_{SS1})\right)\right] \quad (1)$$

where:

q is an electron charge;

k is a Boltzman's constant;

T is an absolute temperature;

n is a constant determined by the configurations of MOS transistors 2a and 2b; and

C is a capacitance of a capacitor 3.

The equation (1) indicates that the sum Of an accumulation value of a photoelectric current I_P and a fixed value determined by $V_{OI} - V_{SS1}$ is logarithmically converted into a voltage V_O. If $V_{OI} - V_{SS1}$ is sufficiently small, the equation (1) can be re-written as:

$$V_0 = V_{SS1} + \frac{nkT}{q} \ln\left(\frac{q}{nkTC}\int I_P dt\right) \quad (2)$$

Thus, the logarithmic conversion of the sum is precisely made.

As described above, according to the prior art (Japanese Patent Application No. H1-334472), the accumulation value of the photoelectric current I_P is logarithmically converted. That is, even if the intensity of light incident onto a photodiode 1 changes during the accumulation and the photoelectric current I_P changes accordingly, the accumulation value of the photoelectric current I_P is logarithmically converted (in a typical solid-state image sensing apparatus which has no logarithmic conversion function, a signal proportional to the accumulation value of the photoelectric current I_P is obtained). With such a feature, a solid-state image sensing apparatus having a wide dynamic range and capable of sensing light from high luminance to low luminance can be realized.

In the prior art, however, when the intensity of light incident onto the photodiode rapidly changes, the output voltage V_O cannot sufficiently follow the change of the light intensity. This results from the fact that a stray capacitance 5 exists at a node 4 of the MOS transistors 2a and 2b as shown by the dotted lines in FIG. 1. That is, in order to obtain the equation (1) or (2), it is necessary, as described in the specification of the prior art, that a gate voltage V_G of the first and second MOS transistors 2a and 2b change in correspondence with the photoelectric current I_P as indicated by the following equation (3):

$$V_G = V_{SS1} + V_T + \left(\frac{nkT}{q} \ln \frac{I_P}{I_{D0}}\right) \quad (3)$$

where:

V_T is a threshold voltage of the first MOS transistor 2a; and

$_{DO}$ is a constant determined by the configuration of the first MOS transistor 2a.

Under a stationary state, the gate voltage V_G is determined by the equation (3) and no currents flow through the stray capacitance 5. However, when the photoelectric current I_P changes, a current for the charging or discharging of the stray capacitance 5 flows through the stray capacitance 5. The current becomes 0 when the charging or discharging is completed, and consequently the gate voltage V_G takes a value obtained by the equation (3). For this reason, the change of the gate voltage V_G is delayed (delayed by the period of time required for the charging or discharging of the stray capacitance 5) compared with the change of the photoelectric current I_P. Hence, when the photoelectric current I_P changes, the logarithmic conversion based on the equation (1) or (2) is not precisely made.

The delay of the change of the voltage V_G will be described in more detail. First, a case will be described where the photoelectric current I_P decreases due to a decrease of the light intensity. In this case, the charge accumulated in the stray capacitance 5 is discharged, so that the potential of the voltage V_G decreases. This discharging is made by means of a drain current of the first MOS transistor 2a. The drain current decreases as the gate voltage decreases. Therefore, the drain current decreases as the drain voltage, i.e. the gate voltage decreases with the proceeding of the discharging of the charge accumulated in the stray capacitance 5. Because of the drain current decrease, the effect of the discharging deteriorates, thereby increasing the discharging time. For this reason, the capability of the gate voltage V_G to follow the change of the photoelectric current I_P deteriorates.

In a case where the photoelectric current I_P increases due to an increase of the light intensity, the potential of the gate voltage V_G increases as charge is accumulated in the stray capacitance 5. The current required for the charging is supplied by the photodiode 1. However, since the current I_P which flows through the photodiode 1 is divided into a current which flows through the stray capacitance 5 and a current which flows through the first MOS transistor 2a, the effect of the charging deteriorates as the current which flows through the first MOS transistor 2a increases. Since the gate of the first MOS transistor 2a is directly connected to the drain thereof, the gate voltage increases as the drain voltage increases, thereby deteriorating the effect of the charging. For this reason, the capability of the gate voltage V_G to follow the change of the photoelectric current I_P deteriorates.

SUMMARY OF THE INVENTION

An object of the present invention is to provide a solid-state image sensing apparatus where an output voltage excellently follows a rapid change of the light intensity, -the dynamic range is therefore wide and light of from high luminance to low luminance can to a high precision be sensed.

To achieve the above-mentioned object, a solid-state image sensing apparatus of the present invention is provided with: means for generating a photoelectric current proportional to an intensity of incident light; a MOS transistor, connected to the generating means, for outputting a signal being logarithmically proportional to the intensity of incident light to the generating means, said MOS transistor being operated in a subthreshold region; and a passive element for connecting a drain and a gate of the MOS transistor.

BRIEF DESCRIPTION OF THE DRAWINGS

This and other objects and features of this invention will become clear from the following description, taken in conjunction with the preferred embodiments with reference to the accompanied drawings in which:

FIG. 1 is a circuit diagram of a conventional solid-state image sensing apparatus;

FIG. 2 is a circuit diagram of a first embodiment of a solid-state image sensing apparatus of the present invention;

FIG. 3 is a circuit diagram of a second embodiment of a solid-state image sensing apparatus of the present invention;

FIG. 4 is a circuit diagram of a third embodiment of a solid-state image sensing apparatus of the present invention;

FIG. 5 is a circuit diagram of a fourth embodiment of a solid-state image sensing apparatus of the present invention; and

FIG. 6 is a circuit diagram of a fifth embodiment of a solid-state image sensing apparatus of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Embodiments of the present invention will hereinafter be described with reference to the drawings.

FIG. 2 shows an arrangement of a circuit corresponding to one pixel of a solid-state image sensing apparatus which is a first embodiment of the present invention. In this circuit, a resistor 8 is inserted between the drain and gate of the first MOS transistor 2a, and the gate of the second MOS transistor 2b is connected to the gate of the first MOS transistor 2a. Stray capacitances 6 and 7 exist at the gate and drain of the first MOS transistor 2a, respectively.

An operation of this circuit in a case where the light intensity rapidly changes will hereinafter be described.

First, a case will be described where the light intensity decreases to decrease the photoelectric current I_P. In this case, the charges accumulated in the stray capacitances 6 and 7 are discharged, respectively, so that the gate voltage V_G and the drain voltage V_D of the first MOS transistor 2a decrease. The discharging of the stray capacitance 7 is made by means of the drain current of the first MOS transistor 2a, while the discharging of the stray capacitance 6 is made by means of the resistor 8 and the drain current of the first MOS transistor 2a.

For the above reasons, the drain voltage V_D of the first MOS transistor 2a decreases by a discharging current i_7 of the stray capacitance 7 While a discharging current i_6 of the stray capacitance 6 is flowing through the resistor 8, the gate voltage V_G is higher than the drain voltage V_D. When the discharging current i_6 becomes 0, the voltage V_G becomes equal to the voltage V_D. In other words, the voltage V_G starts to decrease later than the voltage V_D. Since the drain current is larger the higher the gate voltage V_G is, the drain current does not largely decrease with the proceeding of the discharging of the stray capacitance 7. For this reason, the discharging of the stray capacitance 6 through the resistor 8 is also promptly performed.

In a case where the light intensity increases to increase the photoelectric current I_P, the voltages V_G and V_D increase by the charging of the stray capacitances 6 and 7. In this case, since the current I_P is divided into a charging current supplied to the stray capacitances 6 and 7 and a drain current which flows through the first MOS transistor 2a, the effect of the charging improves as the current which flows through the first MOS transistor 2a decreases. In this embodiment, since the gate of the first MOS transistor 2a is connected to the drain thereof through the resistor 8, the voltage V_G starts to decrease later than the voltage V_D. For this reason, the drain current does not largely increase with the increase of the voltage V_D, and consequently the charging effect of the stray capacitance 7 improves. As a result, the charging of the stray capacitance 6 through the resistor 8 is also promptly performed following the charging of the stray capacitance 7.

FIG. 3 shows a second embodiment of the present invention. This embodiment is different from the first embodiment of FIG. 2 only in that the gate of the second MOS transistor *2b* is directly connected to the drain of the first MOS transistor *2a* and is connected to the gate of the first MOS transistor *2a* through the resistor 8. Other portions are the same as those of FIG. 2.

In this embodiment, the drain voltage of the first MOS transistor *2a* promptly follows the change of the light intensity similarly to the above-described first embodiment. As a result, the output voltage V_O promptly follows the change of the light intensity.

FIG. 4 shows a third embodiment of the present invention. In this embodiment, the resistor 8 of the first embodiment is replaced by a MOS transistor 9, and a direct current voltage V_{GG} is applied to the gate of the MOS transistor 9 through a terminal 10. The conductivity of the MOS transistor 9 can be controlled by controlling the voltage V_{GG}. This indicates that the drain-source of the MOS transistor 9 can equivalently be regarded as a resistor having a value which is in accordance with the voltage V_{GG}. Hence, similarly to the first embodiment, the gate voltage of the first MOS transistor *2a* promptly follows the change of the light intensity, and consequently the output voltage V_O also promptly follows the change of the light intensity.

FIGS. 5 and 6 show fourth and fifth embodiments of the present invention, respectively. In these embodiments, the gate of the MOS transistor 9 of the third embodiment is connected to the drain or the source of the MOS transistor 9. By controlling the threshold voltage of the MOS transistor 9 by means of ion implantation, the same result as that of the third embodiment is obtained. Furthermore, these embodiments are advantageous over the third embodiment in that the terminal 10 for receiving the voltage V_{GG} can be omitted.

Since the first and second MOS transistors *2a* and *2b* operate in the subthreshold region, it is preferable that the MOS transistor 9 also operates in the subthreshold region. In the MOS transistor 9 of the third to fifth embodiments, of the terminal connected to the gate of the first MOS transistor *2a* and the terminal connected to the drain of the first MOS transistor *2a* as described above, the terminal having a lower potential functions as the source and the terminal having a higher potential functions as the drain. Since the source of the MOS transistor 9 is connected to the drain or the gate of the first MOS transistor *2a*, the substrate bias voltage of the MOS transistor 9 is higher than that of the first MOS transistor *2a*. For this reason, in order to cause the MOS transistor 9 to operate in the subthreshold region, it is necessary to determine the threshold voltage of the MOS transistor 9 so as to be lower than that of the first MOS transistor *2a*. Such a threshold voltage can be realized by the ion implantation of phosphorus into the gate region of the MOS transistor 9.

While n-channel MOS transistors are employed as the first and second MOS transistors *2a* and *2b* in the above-described embodiments, p-channel MOS transistors may be employed (although it is necessary to change the bias relationship). Moreover, while the gate of the second MOS transistor *2b* is connected to the gate of the first MOS transistor *2a* in the third to fifth embodiments, it is clear that the same result is obtained even if the gate of the second MOS transistor *2b* is connected to the drain of the first MOS transistor *2a*.

Obviously, many modifications and variations of the present invention are possible in light of the above teachings. It is therefore to be understood that within the scope of the appended claims, the invention may be practiced other than as specifically described.

What is claimed is:

1. An image sensing device comprising:
   - means for generating a photoelectric current proportional to an intensity of incident light;
   - a first MOS transistor, connected to the generating means, for outputting a signal which is logarithmically proportional to the intensity of incident light to the generating means, said first MOS transistor is operated in a subthreshold region; and
   - an active element, connecting a drain and a gate of the first MOS transistor, for delaying a variation in gate voltage of the first MOS transistor, said voltage variation being brought about by a variation in the photoelectric current
   - wherein any stray capacitance existing at the gate of the first MOS transistor is promptly charged or discharged through the active element.

2. An image sensing device as claimed in claim 1, wherein the active element is a second MOS transistor different from the first MOS transistor.

3. An image sensing device as claimed in claim 2, wherein a direct-current voltage is applied to a gate of the second MOS transistor.

4. An image sensing device as claimed in claim 2, wherein a gate of the second MOS transistor is connected to a drain or a source of the second MOS transistor.

5. An image sensing device as claimed in claim 2, wherein the second MOS transistor is operated in a subthreshold region.

6. An image sensing device as claimed in claim 1, further comprising:
   - a third MOS transistor being operated in the subthreshold region, and being connected to the gate and the drain of the first MOS transistor with a gate of the third MOS transistor; and
   - a capacitor being connected to a source of the third MOS transistor;
   - wherein a voltage resulting from a connection between the source of the third MOS transistor and the capacitor is logarithmically proportional to an integrated amount of the photoelectric current.

7. An image sensing device responsive to a rapidly changing light intensity, comprising:
   - means for generating a photoelectric current proportional to an intensity of incident light;
   - an MOS transistor, having a gate forming an output and a drain, connected to the generating means, for outputting at the output a signal logarithmically proportional to the intensity of incident light to the generating means, the MOS transistor is operated in a subthreshold region;
   - means for maintaining the gate voltage at a higher voltage than the drain voltage during any rapid light intensity change, the maintaining means enabling a prompt charging or discharging of any stray capacitance generated by the rapid change in light intensity, the stray capacitance having a voltage at the output;
   - circuitry for receiving the voltage from the stray capacitance, the voltage reflecting the prompt charge or discharge of the stray capacitance.

8. An image sensing device responsive to rapidly changing light intensity, comprising:

means for generating a photoelectric current proportional to an intensity of incident light;

a first MOS transistor, having a gate and a drain, connected to the generating means for outputting a signal logarithmically proportional to the intensity of incident light to the generating means, the MOS transistor is operated in a subthreshold region; and

means for delaying a variation in gate voltage to enable a prompt charging or discharging of any stray capacitance generated by the rapid change in light intensity, the delaying means comprising:

a second MOS transistor, connected between the gate and drain of the first MOS transistor; and

a voltage source applying a voltage to the second MOS transistor of a magnitude to permit the gate voltage of the first MOS transistor to promptly follow any change in intensity of incident light, thereby allowing the second MOS to accurately follow rapid changes in light intensity.

* * * * *

In IDS

US005241575A

United States Patent [19]

Miyatake et al.

[11] Patent Number: 5,241,575

[45] Date of Patent: Aug. 31, 1993

[54] SOLID-STATE IMAGE SENSING DEVICE PROVIDING A LOGARITHMICALLY PROPORTIONAL OUTPUT SIGNAL

[75] Inventors: Shigehiro Miyatake, Osaka; Kenji Takada, Neyagawa; Jun Hasegawa, Minamiashigara; Yasuhiro Nanba, Toyonaka, all of Japan

[73] Assignee: Minolta Camera Kabushiki Kaisha, Osaka, Japan

Fig 6 has a controller for resetting potential at the 1st transistor by switching Voltage applied to the Control Electrode of the 1st transistor

[21] Appl. No.: 942,349

[22] Filed: Sep. 9, 1992

Related U.S. Application Data

[63] Continuation of Ser. No. 630,307, Dec. 19, 1990, abandoned.

[30] Foreign Application Priority Data

Dec. 21, 1989 [JP] Japan 1-334472

[51] Int. Cl.[5] H01L 29/78; H01L 27/14; H01L 31/00

[52] U.S. Cl. 377/60; 377/62; 257/226; 257/234; 257/236; 257/292; 257/448; 257/462; 257/901; 307/308; 307/311; 307/571; 307/580

[58] Field of Search 357/30; 257/290, 292, 257/443, 448, 461, 462, 901, 226, 234, 236; 307/580, 308, 311, 571; 377/60, 62

[56] References Cited

U.S. PATENT DOCUMENTS

4,085,411	4/1978	Genesi	307/311
4,384,300	5/1983	Iizuka	307/291
4,447,746	5/1984	Fang et al.	257/290
4,473,836	9/1984	Chamberlin	357/30
4,584,606	4/1986	Nagasaki	358/209
4,598,414	7/1986	Dries et al.	377/58
4,742,238	5/1988	Sato	250/578
4,742,380	5/1988	Chang et al.	357/30
4,745,446	5/1988	Cheng et al.	357/30
4,791,396	12/1988	Nishizawa et al.	357/30
4,841,349	7/1989	Nakano	357/30
4,845,355	7/1989	Nakagawa et al.	357/30
4,857,725	8/1989	Goodnough et al.	307/311
4,901,129	2/1990	Hynecek	357/30
4,973,833	11/1990	Takada et al.	250/208.1
4,990,981	2/1991	Tanaka et al.	357/30
5,034,625	7/1991	Min et al.	307/296.2
5,136,184	8/1992	Deevy	307/491

FOREIGN PATENT DOCUMENTS

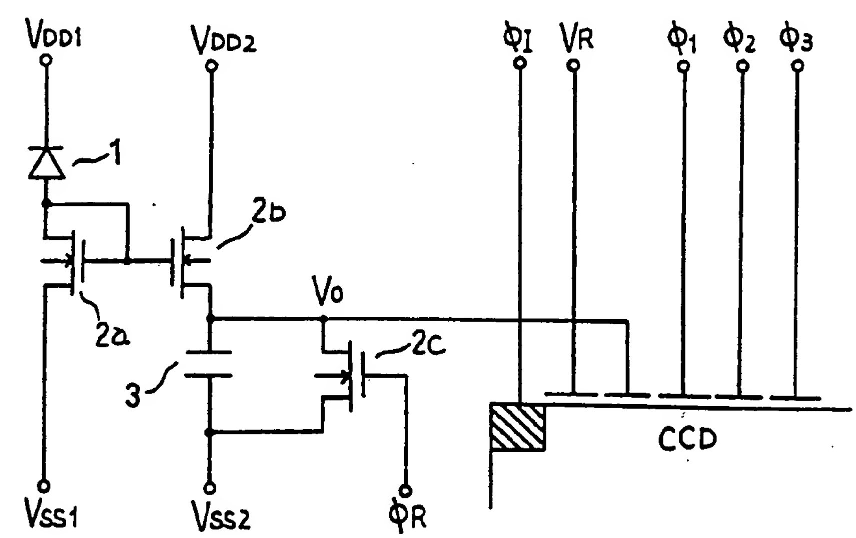
1-253960 10/1989 Japan .

Primary Examiner—Andrew J. James
Assistant Examiner—Ngan Van Ngo
Attorney, Agent, or Firm—Price, Gess & Ubell

[57] ABSTRACT

An image sensing device that outputs a signal logarithmically proportional to the intensity of the incident light. The image sensing device makes use of a sub-threshold current flowing between the drain and source of a MOS transistor when the gate voltage is below the threshold voltage (above which the MOS transistor is nominally conductive and below which nominally non-conductive). Since the logarithmic conversion is done in the photosensing section of a solid-state image sensing device, the output from the device is already compressed and is easily handled by a small capacity CCD. Some output systems for the image sensing device of the present invention are also described.

4 Claims, 7 Drawing Sheets



11/17/2003, EAST Version: 1.4.1

FIG. 1

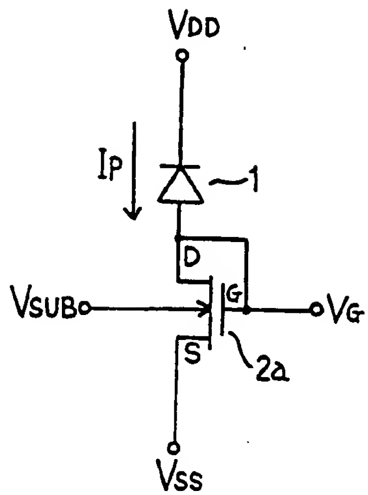

VDD
IP
1
D
G
VSUB
VG
S
2a
VSS

FIG. 2

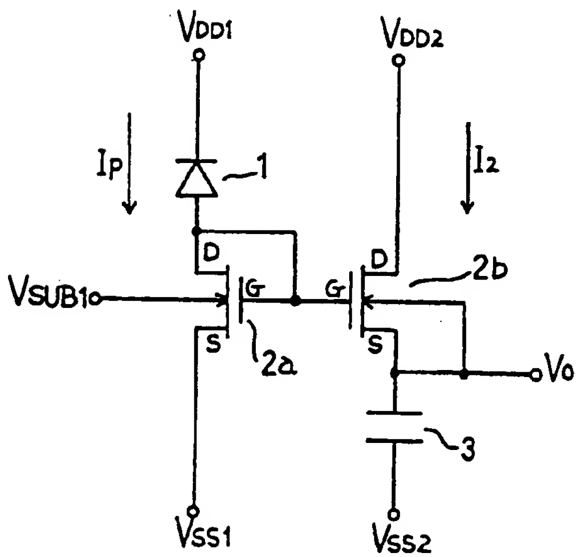

VDD1
VDD2
IP
1
I2
D
D
2b
VSUB1
G
G
S
S
2a
VO
3
VSS1
VSS2

FIG. 3A

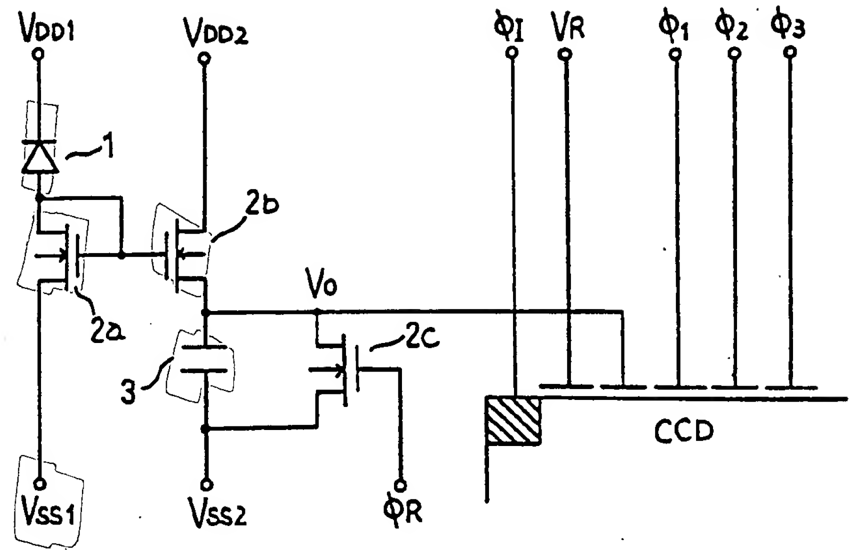
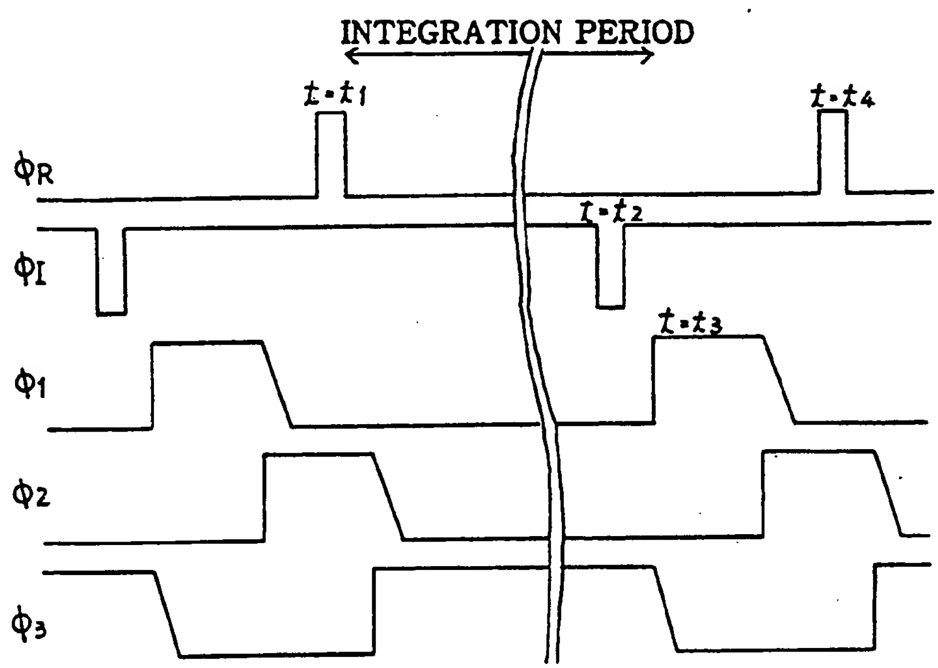

VDD1
VDD2
1
2b
2a
Vo
2c
3
Vss1
Vss2
φR
φI
VR
φ1
φ2
φ3
CCD

FIG. 3B


INTEGRATION PERIOD
t=t1
t=t2
t=t3
t=t4
φR
φI
φ1
φ2
φ3

Shows Reset transistor and low pulse through the second transistor are equivalent

FIG. 4A

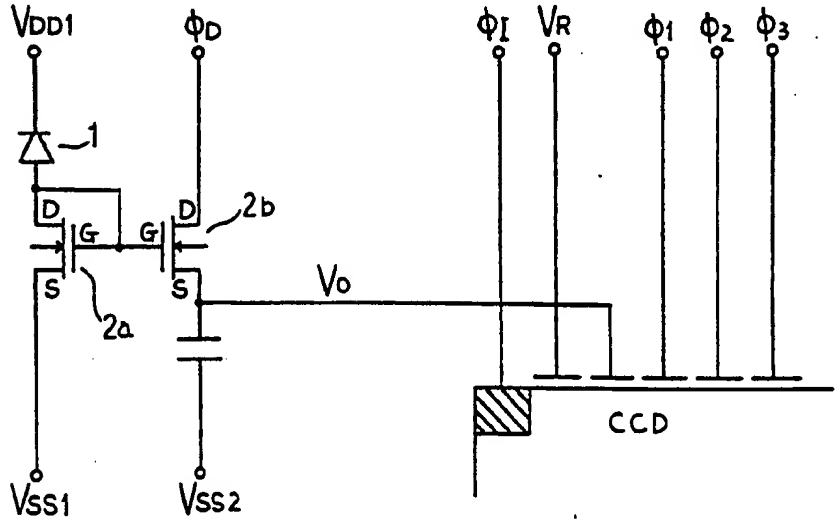


FIG. 4B

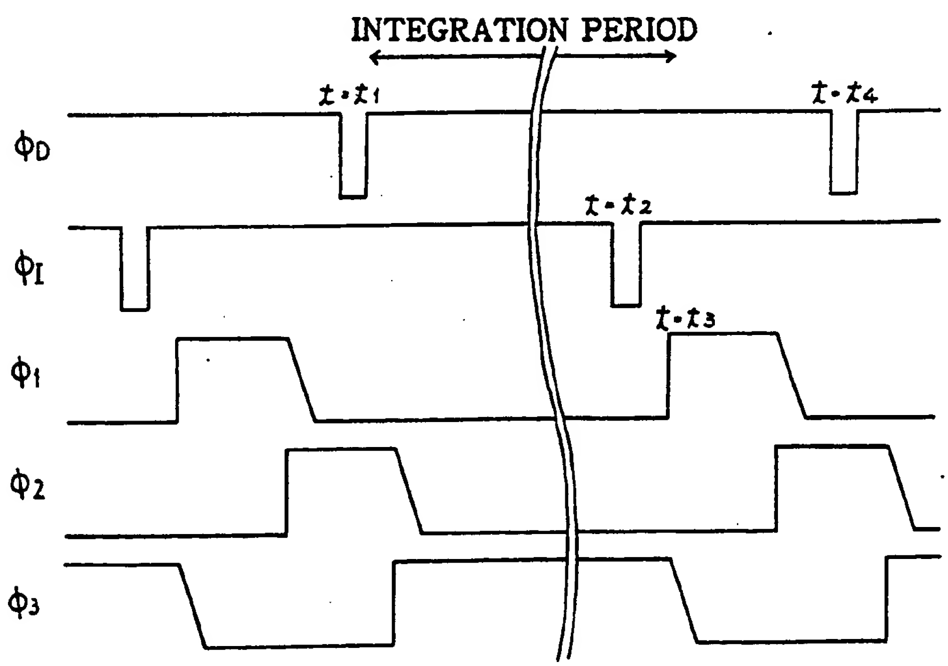


FIG. 5A

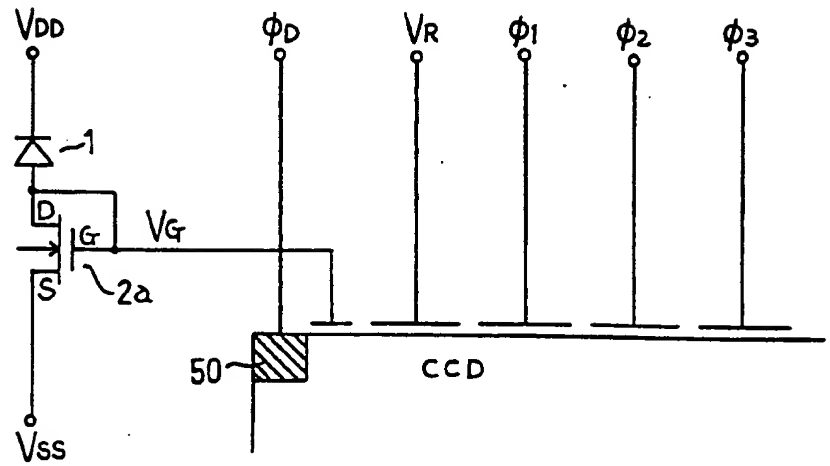

VDD
1
D
G
VG
S
2a
Vss
φD
VR
φ1
φ2
φ3
50
CCD

FIG. 5B

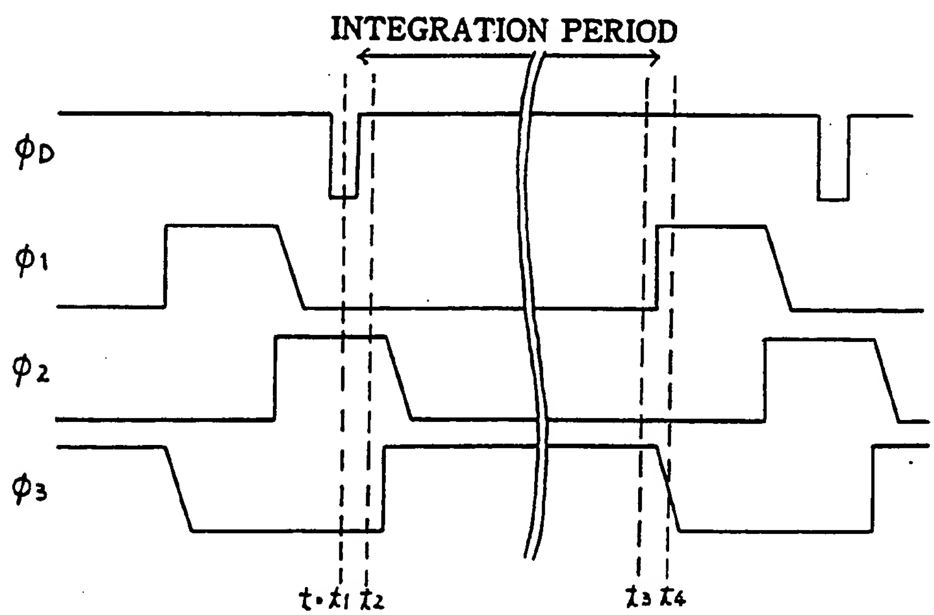
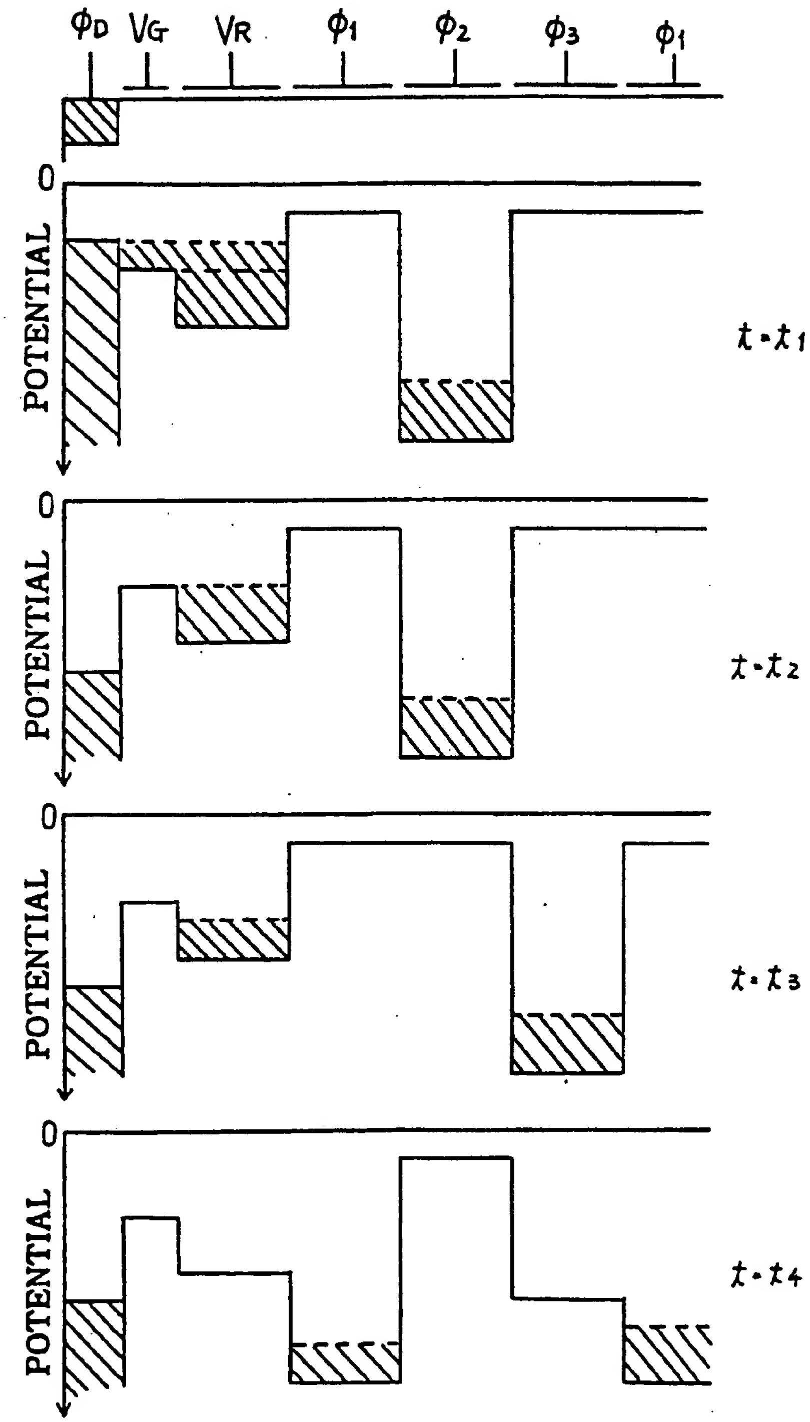

INTEGRATION PERIOD
φD
φ1
φ2
φ3
t0 t1 t2
t3 t4

FIG. 5C



ΦD
VG
VR
Φ1
Φ2
Φ3
Φ1
0
POTENTIAL
t=t1
0
POTENTIAL
t=t2
0
POTENTIAL
t=t3
0
POTENTIAL
t=t4

FIG. 6

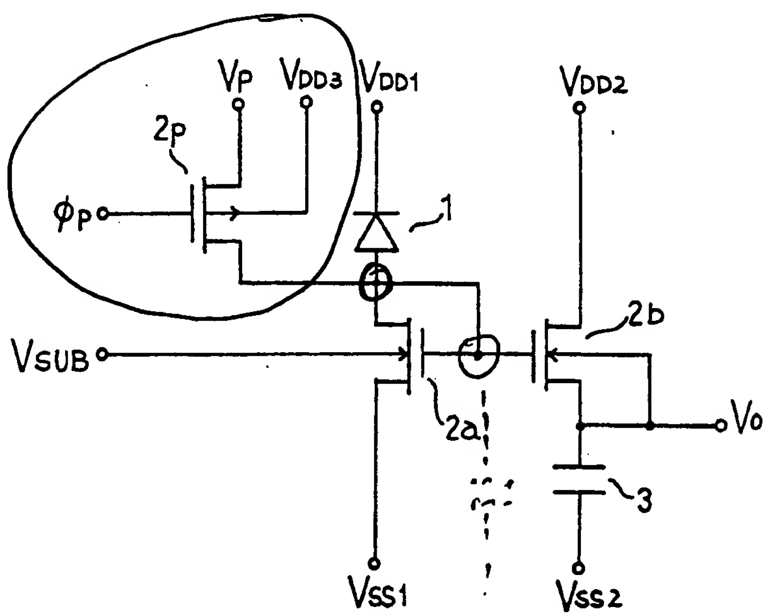


FIG. 7A

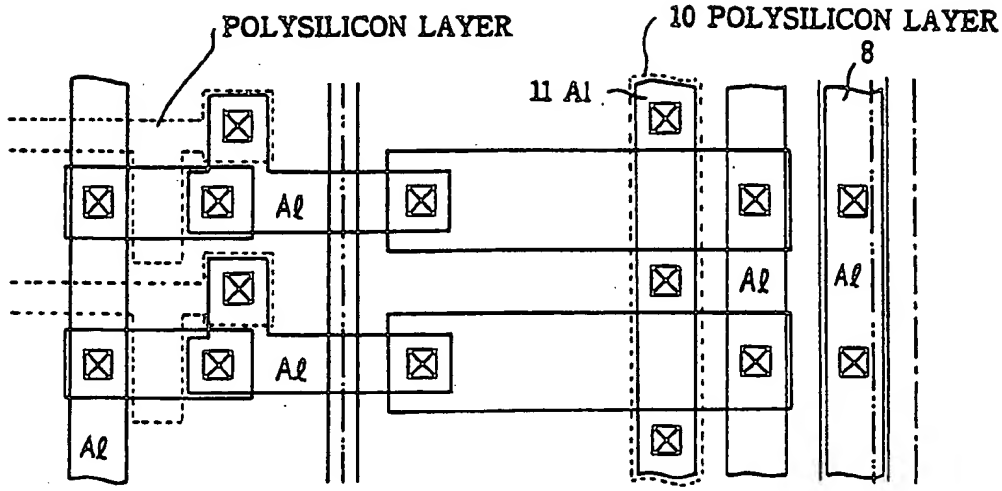


FIG. 7B

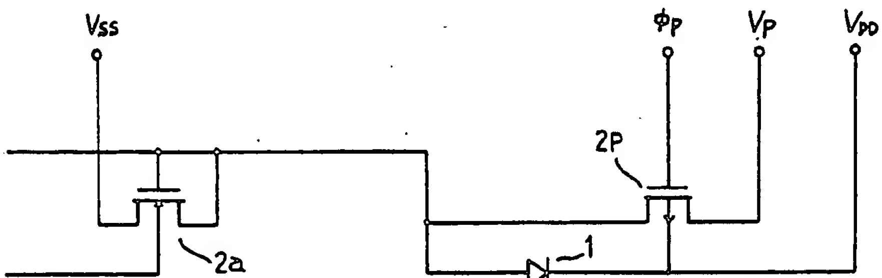
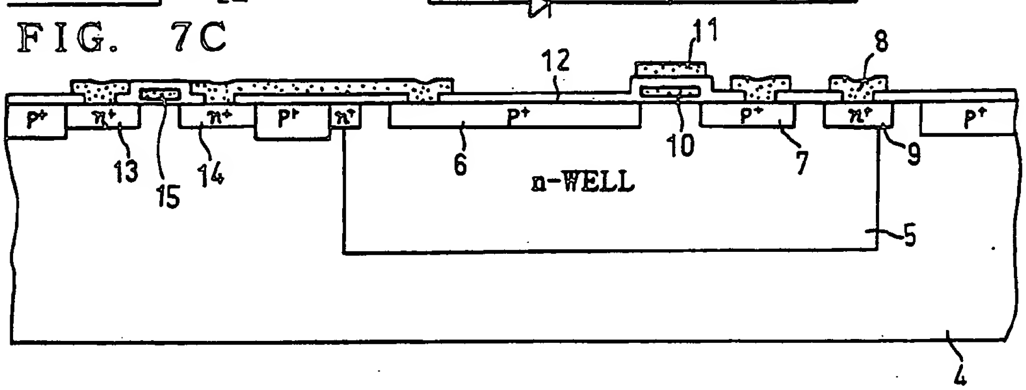


FIG. 7C



SOLID-STATE IMAGE SENSING DEVICE PROVIDING A LOGARITHMICALLY PROPORTIONAL OUTPUT SIGNAL

This is a continuation of application Ser. No. 07/630,307 filed on Dec. 19, 1990 now abandoned.

BACKGROUND OF THE INVENTION

The present invention relates to a solid-state image sensing device, i.e., a device that converts light into electrical signal, especially a non-linear image sensing device whose conversion characteristic is compressive.

Solid-state image sensing device can be very small, light-weight and consumes less power. It has further advantages such that it is free from distortion in the image field and robust against sticking, vibration or strong external magnetic field. Since the solid-state chip can be manufactured by the same or similar process as that of general LSIs (Large Scale Integrated circuits), it can be mass-produced with high reliability. Thus, solid-state image sensing devices are widely used in many fields: for example, a linear image sensing device is used in a tele-facsimile machine and a two-dimensional image sensing device is used in a video recorder.

One of few shortcomings of the solid-state image sensing device is that the dynamic range is relatively small compared to the normal chemical photographic film using silver salt. This necessitates a subtle control of the exposure (light amount inputted into the solid-state image sensing device). Even using a sophisticated exposure control, there are sometimes the case where the dark part of the image is sensed completely black and the bright part of the image is sensed completely white (the output from the image sensing device saturates).

SUMMARY OF THE INVENTION

An object of the present invention is therefore to provide a solid-state image sensing device having a wide dynamic range.

Another object of the present invention is to make the solid-state image sensing device as small as possible so that it can be used in a compact-size video camera etc.

These and other objects are achieved by an image sensitive device of the present invention comprising: a MOS transistor having a gate, a source and a drain formed on a substrate; connecting means for electrically connecting the gate and the drain; photoelectric current generating means (such as a photodiode) for generating a photoelectric current proportional to an intensity of incident light, where the current is provided to the drain of the MOS transistor; and means for applying a voltage to the substrate of the MOS transistor in order to keep the voltage of the gate below a threshold voltage above which the MOS transistor becomes conductive between the source and the drain. The image sensitive device of the present invention is further characterized by that it outputs a signal logarithmically proportional to the intensity of light incident to the photoelectric current generating means.

Another feature of the present invention is an image sensitive device comprising: photosensitive means (such as a photodiode) for generating photoelectric current proportional to an intensity of incident light; logarithmic means for receiving the photoelectric current and generating a signal logarithmically proportional to the photoelectric current, the logarithmic means including a first MOS transistor having a gate, a source and a drain formed on a substrate; and integrating means for receiving the signal and integrating the signal for a preset period.

Other features of the present invention and specific examples of every means constituting above features of the invention is described in detail in the description of the embodiments that follow.

BRIEF DESCRIPTION OF THE ATTACHED DRAWINGS

FIG. 1 is a circuit diagram of an image sensing device as the first embodiment of the present invention.

FIG. 2 is a circuit diagram of an image sensing device as the second embodiment of the present invention.

FIG. 3A is a construction diagram of the first example of an output system for the image sensing device of the second embodiment where the output signal is given to a CCD, and FIG. 3B is a timing chart of the driving signals for the CCD.

FIG. 4A is a construction diagram of the second example of an output system for the image sensing device of the second embodiment where the output signal is given to a CCD, and FIG. 4B is a timing chart of the driving signals for the CCD.

FIG. 5A is a construction diagram of the third example of an output system for the image sensing device of the second embodiment where the output signal is given to a CCD, FIG. 5B is a timing chart of the driving signals for the CCD, and FIG. 5C shows potential diagrams at different stages of the charge transfer in the CCD.

FIG. 6 is a circuit diagram of an image sensing device added a pre-charge circuit to the circuit of the second embodiment.

FIG. 7A is an example of concrete structure of the image sensing device of the circuit as shown in FIG. 6, FIG. 7B is the circuit diagram, and FIG. 7C is the cross-sectional view of the structure.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Before describing an embodiment of the present invention, the principle of the logarithmic compression used in the present invention is explained.

In case of a MOS (Metal Oxide Semiconductor) transistor, a small amount of current ("sub-threshold current") flows under the gate when the gate voltage is lower than the so-called threshold voltage of the MOS transistor above which the MOS transistor becomes nominally conductive between the drain and the source and below which the MOS transistor becomes nominally non-conductive. The sub-threshold current is due to a weak inversion state occurring in the surface area of the silicon substrate under the gate oxide layer, and the sub-threshold current causes various deleterious effects and therefore is thought to be undesirable characteristic of MOS transistors. The present invention uses the sub-threshold current to control the photoelectric conversion characteristic of the solid-state image sensing device.

The amount of the sub-threshold current is calculated as follows (cf. R. M. Swanson and J. D. Meindl, "Ion-implanted Complementary MOS Transistors in Low-voltage Circuits", IEEE Journal of Solid-State Circuits, Vol. SC-7, No. 2, pp. 146-153, April, 1972). When $V_G - V_S \leqq V_T + n(kT/q)$ applies, the drain current I_D of an n-channel MOS transistor is:

$$I_D=(Z/L)\mu_n C_o(1/m)(nkT/q)^2\exp\{(q/nkT)(V_G-V_S-V_T-nkT/q)\}\cdot\{1-\exp((-mq/nkT)(V_D-V_S))\} \quad (1)$$

where

V_G, V_D, V_S, V_T: gate, drain, source and threshold voltages of the MOS transistor,
Z: channel width of the MOS transistor,
L: channel length of the MOS transistor,
μ_n: electron mobility,
q: charge of an electron,
k: Boltzman's constant,
T: absolute temperature, and
C_o: capacitance of the gate insulation layer.

In equation (1),

$m=(C_o+C_d)/C_o$
$n=(C_o+C_d+C_{fs})/C_o$
$C_{fs}=qN_{fs}$

where

C_d: capacitance of the depletion layer, and
N_{fs}: surface state density.

When N_{fs} is 0, m equals n. If $V_D-V_S>>kT/q$, and the drain current I_D of equation (1) will be:

$$I_D=I_{DO}\exp\{(q/nkT)(V_G-V_S-V_T)\} \quad (2)$$

where

$$I_{DO}=(Z/L)\mu_n C_o(1/n)(nkT/q)^2\exp(-1) \quad (3)$$

Equation (2) indicates that the drain current I_D is a function of the gate-source voltage (V_G-V_S) when $V_G-V_S \leqq V_T+n(kT/q)$ and $V_D-V_S>>kT/q$.

The solid-state image sensing device of the present invention makes use of the minute sub-threshold current of the MOS transistor. The first embodiment of the invention is now described referring to FIG. 1. FIG. 1 is a circuit diagram showing one pixel of the solid-state image sensing device. The pn-junction photodiode 1 is the photosensitive element, whose anode is connected to the drain D and gate G of an n-channel MOS transistor 2a. The cathode of the photodiode 1 is connected to a direct current (DC) source V_{DD}, the source S of the MOS transistor 2a is to another DC source V_{SS}, and the back gate (substrate) of the MOS transistor is to a third DC source V_{SUB}. Here $V_{DD}>V_{SS}\geqq V_{SUB}$, i.e., the photodiode 1 is applied a reverse bias and the drain D and source S of the MOS transistor is also applied a reverse bias as to the substrate.

When light is irradiated onto the photodiode 1, photocurrent I_P proportional to the intensity of the input light flows from the cathode to the anode of the photodiode 1. Since $V_D=V_G$,

$$kT/q<<V_G-V_{SS}\leqq V_T+nkT/q \quad (4)$$

Hence, the current I_D flowing through the MOS transistor 2a is

$$I_D=I_{DO}\exp\{(q/nkT)(V_G-V_{SS}-V_T)\} \quad (5)$$

Since I_D equals I_P in a steady state,

$$I_P=I_{DO}\exp\{(q/nkT)(V_G-V_{SS}-V_T)\} \quad (6)$$

Hence,

$$V_G=V_{SS}+V_T+(nkT/q)\ln(I_P/I_{DO}) \quad (7)$$

which means that the gate voltage V_G represents the logarithmic value of the photocurrent I_P.

The inequality (4) can be satisfied by adjusting the substrate voltage V_{SUB} as follows. Equation (2) shows that the drain current I_D is a function of the threshold voltage V_T, and the threshold voltage V_T is given by:

$$V_T=\Phi_{MS}-qN_{fs}/C_o+\Phi_f+\{2\epsilon_{SI}\epsilon_o qN_B(|2\Phi_f|+V_S-V_{SUB})\}^{\frac{1}{2}}/C_o \quad (8)$$

where

Φ_{MS}: difference in the work function of the gate electrode and the silicon substrate,
Φ_f: Fermi level of the silicon substrate,
ϵ_{SI}: specific dielectric constant of the silicon substrate,
ϵ_o: dielectric constant of the vacuum, and
N_B: impurity density in the silicon substrate.

Equation (8) shows that the threshold voltage V_T changes according to $V_{SS}-V_{SUB}(=V_S-V_{SUB})$. Since the drain current I_D changes according to the threshold voltage V_T, the substrate voltage V_{SUB} can be properly adjusted to satisfy the inequality (4).

A specific example of the image sensing device is now described. The constants of the example are as follows:

$N_B=1\times10^{15}/cm^3$
$Z/L=1$
$\mu_n=1000\ cm^2/V\cdot sec$
$T=300K$
$C_o=3.5\times10^{-8}F/cm^2$

If the gate electrode is made of aluminum, $\Phi_{MS}=-0.9$ V at the impurity density N_B of the substrate. Suppose, for simplicity, C_d, C_{fs} and N_{fs} are all 0 ($C_d=C_{fs}=0$, $N_{fs}=0$), both m and n equal 1 (m=n=1). In this case, I_{DO} is

$$I_{DO} = 1000\times3.5\times10^{-8}\times0.026^2\times0.368$$
$$= .8.70\times10^{-9}$$

and the threshold voltage V_T is, when $V_S-V_{SUB}=0$ V,

$$V_T(0)=-0.9+0.58+(2\times11.7\times8.85\times10^{-14}\times1.6\times10^{-19}\times10^{15}\times0.58)^{\frac{1}{2}}/3.5\times10^{-8}=0.08$$

and when $V_S-V_{SUB}=5$ V,

$$V_T(5)=0.91$$

When the luminance on the surface of the photosensitive element (photodiode 1) is in the range between 0.1 1× and 10^4 1×, the photocurrent I_P is approximately from 10^{-14} to 10^{-9} A, if the area of the photosensitive element is 100 μm^2. From equation (7), the value of (V_G-V_{SS}) is between $(V_T-0.06)$ to $(V_T-0.36)$. Specifically,

when $V_S-V_{SUB}=0$ V, $V_G-V_{SS}=0.02$ to -0.28

when $V_S-V_{SUB}=5$ V, $V_G-V_{SS}=0.85$ to 0.55

which shows that the inequality (4) is not satisfied when $V_S-V_{SUB}=0$ V but is satisfied when $V_S-V_{SUB}=5$ V. Thus it is proved that by properly adjusting the substrate voltage V_{SUB}, the value of the photocurrent I_P can be converted into logarithmically compressed voltage value.

FIG. 2 shows another embodiment of the present invention in which an integral circuit is added to the

first embodiment shown in FIG. 1. Here also the pn-junction photodiode 1 is the photosensitive element, and the anode of the photodiode 1 is connected to the drain and gate of a first n-channel MOS transistor 2a and the gate of a second n-channel MOS transistor 2b. DC voltage V_{DD1} is applied to the cathode of the photodiode 1, V_{SS1} to the source of the first MOS transistor 2a, V_{DD2} to the drain of the second MOS transistor 2b. The source of the second MOS transistor 2b is connected via a capacitor 3 (capacitance=C) to a DC source V_{SS2}. To the substrate of the first MOS transistor 2a is connected a DC source V_{SUB1}. When the second MOS transistor 2b is formed on the same chip, or in the same well, as the first MOS transistor 2a, the substrate of the second MOS transistor 2b is applied the same voltage V_{SUB1}. When the second MOS transistor 2b is formed on a separate chip, or in a different well, from the first MOS transistor 2a, a different DC source V_{SUB2} is applied to the substrate of the second MOS transistor 2b or the substrate is connected to the source of the MOS transistor 2b.

In this embodiment, as described below, the integral value of the photocurrent I_P is logarithmically compressed and the compressed value is obtained as the voltage V_o at the junction of the source of the second MOS transistor 2b and the capacitor 3.

In the following calculations, it is supposed that the characteristics of the first MOS transistor 2a and of the second MOS transistor 2b are the same, and the substrate of the second MOS transistor 2b is connected to its source. The voltage V_G commonly applied to the gates of the first and second MOS transistors 2a and 2b is given as:

$$V_G=V_{SS1}+V_T+(nkT/q)\ln(I_P/I_{DO}) \tag{9}$$

and the current I_2 flowing through the second MOS transistor 2b is, from equation (2):

$$I_2=I_{DD}\exp\{(q/nkT)(V_G-V_o-V_T)\} \tag{10}$$

Further,

$$I_2=C(dV_o/dt) \tag{11}$$

From equations (9), (10) and (11),

$$C(dV_o/dt)=I_P\exp\{(q/nkT)(V_{SS1}-V_o)\}$$

or

$$\exp\{(q/nkT)(V_o-V_{SS1})\}dV_o=(I_P/C)dt \tag{12}$$

Integrating the equation (12) with the condition that $V_o=V_{o1}$ at $t=0$,

$$V_o=V_{SS1}+(nkT/q)\ln[(q/(nkTC))\int I_Pdt+\exp\{(q/nkT)(V_{o1}-V_{SS1})\}] \tag{13}$$

Equation (13) indicates that the sum of the integral value of the photocurrent I_P and a constant value determined by $V_{o1}-V_{SS1}$ is logarithmically converted. Since the constant value $\exp\{(q/nkT)(V_o-V_{SS1})\}$ decreases as $V_{o1}-V_{SS1}$ decreases, the logarithmic conversion can be more accurate when the initial value V_{o1} of the voltage V_o is set smaller compared to the source voltage V_{SS1} of the first MOS transistor 2a.

The output voltage generated by the above described circuits can be given as charges to a CCD by the voltage balancing method (cf. Carlo H. Sequin and Michael F. Tompsett, Bell Telephone Laboratory. *Charge Transfer Devices*, New Jersey: Murray Hill) or other methods. In this case, after the charges are transferred to the CCD and the initial value of the voltage V_o is set at V_{o1}, another round of integration should be started again. FIGS. 3A-4B show the circuits and timing charts for the output process. The pulse timing in the timing charts is based on the charge balancing method.

In FIG. 3A, a third MOS transistor 2c is used to reset the capacitor 3. In FIG. 4A, no additional transistor is used but pulse signal is given to the drain of the second MOS transistor 2b. In any case, three-phase-driven CCD is used, i.e., three pulse signals Φ_1, Φ_2 and Φ_3 are used to transfer charges. The signal charges are injected by the difference in the voltage of the electrode applied V_R (a DC voltage) and the electrode applied V_o.

The operation of the injection and transfer is now explained. When Φ_R becomes high (in case of FIGS. 3A and 3B) or Φ_D becomes low (in case of FIGS. 4A and 4B) at $t=t_1$, the voltage V_o is set at the value V_{SS2}. Then the voltage V_o increases according to the equation (13) (where $V_{o1}=V_{SS2}$). When Φ_1 becomes low at $t=t_2$, electrical charges proportional to the value of V_o-V_R are stored under the electrode applied V_o. When Φ_1 becomes high at $t=t_3$, the stored charges are transferred under the electrode applied Φ_1. Similarly, as the drive pulses Φ_2 and Φ_3 become high, the signal charges are transferred through the corresponding electrodes. When Φ_R returns low (in case of FIGS. 3A and 3B) or Φ_D returns high (in case of FIGS. 4A and 4B) at $t=t_4$, the voltage V_o is again reset at the value V_{SS2} and a new round of charge integration starts. Thus the logarithmically compressed signal is injected as signal charges into CCD and transferred in the CCD.

FIGS. 5A, 5B and 5C show still another circuit for the charge injection of the logarithmically compressed output signal. In this embodiment, the second MOS transistor 2b in FIGS. 3A and 4A is combined with the CCD. That is, as shown in FIG. 5A, the cathode of the pn-junction photodiode 1 is applied a DC voltage V_{DD}, and the anode of the photodiode 1 is connected to the gate and drain of the sole MOS transistor 2a and the first electrode of the CCD. DC voltage V_{SS} is applied to the source of the MOS transistor 2a and V_R is applied to the second electrode of the CCD. To the third electrode of the CCD is applied Φ_1, to the fourth, Φ_2, to the fifth, Φ_3, and so on. To the input diode 50 of the CCD is applied Φ_D pulse.

Referring to the timing chart of these pulse signals in FIG. 5B and the potential diagram in FIG. 5C, the operation of the output circuit is now explained. When the pulse signal Φ_D becomes low at $t=t_1$, the electrons are injected into the region under the electrode V_R through the region under the electrode V_G. When the pulse signal Φ_D becomes high at $t=t_2$, the excessive electrons return to the input diode. These are the resetting operation, and then a new round of integration starts. At this condition, the electrons under the electrode V_R are drained through the region under the electrode V_G to the input diode 50. This means that a current flows from the input diode 50 to the region under the electrode V_R, and the amount of the current is the exponential function of the voltage difference between V_G and V_R. In this embodiment, the input diode 50 of the CCD corresponds to the drain of the second MOS transistor 2b and in FIG. 4A, and the electrons stored under the second gate of the CCD

correspond to the charges stored in the capacitor connected to the source of the second MOS transistor 2b and in the source of the second MOS transistor 2b. After the integration is finished at $t=t_3$, the pulse signal Φ_1 becomes high at $t=t_4$ and the electrons stored under the electrode V_R are transferred to the CCD.

The high speed operation of the embodiment is now explained. A stray capacitance exists around the gate of the first MOS transistor 2a. In order to cope with a high speed operation and adequately follow the change in the photocurrent I_P, the stray capacitance must charge or discharge in a sufficiently short time compared to the integration time. Since the gate and the drain are connected to each other in the first MOS transistor 2a in FIG. 2, the discharging of the stray capacitance (where the photocurrent I_P changes from a larger value to a smaller value) is done by the first MOS transistor 2a. But the charging of the stray capacitance (where the photocurrent I_P changes from a smaller value to a larger value) must be done by the photocurrent I_P, which takes longer time than in the case of charging.

The embodiment shown in FIG. 6 addresses the problem, where a pre-charge transistor 2p is added. The pre-charge transistor 2p is connected to the gate of the first MOS transistor 2a. Before starting an integration, the pre-charge transistor 2p is turned on (i.e., become conductive) by a pre-charge pulse Φ_P, whereby the voltage at the gate of the first MOS transistor 2a becomes high. When the integration starts, the first MOS transistor 2a is in a discharging state and the proper gate voltage corresponding to the photocurrent can be obtained at a shorter time.

In FIGS. 7A-7C, the pre-charge transistor 2p in FIG. 6 is realized by a p-channel MOS transistor. In this specific example, the drain of a p-channel MOS transistor is used as the anode of a photodiode. The structure of the example is as follows. In a p-substrate 4, an n-well region 5 is formed, which will be the cathode of a photodiode 1. On the n-well region 5, a P^+-region 6 is formed by the diffusion method, which will be the anode of the photodiode. A p-channel MOS transistor 2p is formed on the n-well region 5, where the P^+-region 6 (which is used as the anode of the photodiode) is used also as the drain of the p-channel MOS transistor 2p. Another P^+-region 7 is formed on the n-well region 5, and is used as the source of the p-channel MOS transistor 2p. A DC voltage V_{DD} is applied to the n-well 5 through an aluminum electrode 8 and an n^+-region 9, DC voltage V_P is applied to the source 7 of the p-channel MOS transistor 2p, and a pre-charge pulse signal Φ_P is input into the gate of the transistor 2p through an appropriate electrode 10. On other regions of the substrate 4 are formed an n-channel MOS transistor 2a (with a source 13 and drain 14 formed by n^+-regions and a gate 15 therebetween) and a CCD. Here the circuit as shown in FIGS. 1-5A is completed. An aluminum line 11 is placed (via an insulation layer 12) on the gate electrode 10 in order to decrease the resistance of the gate line which is formed by polysilicon.

As described above in detail, the image sensing device according to the present invention can generate an electrical signal whose value is proportional to the logarithm of the intensity of input light. That is, the large dynamic range of the input light is effectively compressed to become a smaller signal output range. Since the logarithmic compression is performed in the photoelectric converting section of the image sensing device, the overall dynamic range of the image sensing device is not restricted by the dynamic range of the signal transfer section that transfers the signal charges to the output terminal of the device. Further, the image sensing device of the present invention can be highly integrated because the device uses MOS transistors, and it is still possible to form a CCD on the same chip.

What is claimed is:

1. An image sensitive device, comprising:

a first MOS transistor having a gate, a source and a drain, said first MOS transistor operating in a subthreshold region;

a second MOS transistor having a gate, a source and a drain, said second MOS transistor operating in a subthreshold region, and said gate of the second MOS transistor being connected to the gate and drain of the first MOS transistor;

photoelectric current generating means for generating a photoelectric current proportional to an intensity of incident light, said photoelectric current being provided to the drain of the first MOS transistor; and

a capacitor connected to the source of the second MOS transistor; wherein a voltage resulting from a connection between the source of the second MOS transistor and the capacitor is logarithmically proportional to an integrated amount of the photoelectric current.

2. An image sensitive device as claimed in claim 1, wherein a pulse signal is applied to the drain of the second MOS transistor so that the second MOS transistor initializes the voltage of the connection between the source of the second MOS transistor and the capacitor.

3. An image sensitive device, comprising:

a MOS transistor having a gate, a source and a drain, said MOS transistor operating in a subthreshold region;

photoelectric current generating means for generating a photoelectric current proportional to an intensity of incident light, said photoelectric current being provided to the drain of the MOS transistor;

a charge-coupled device whose first gate is connected to the gate and drain of the MOS transistor; and

means for applying a direct-current voltage to a second gate of the charge-coupled device; wherein an amount of charge stored under the second gate of the charge-coupled device is logarithmically proportional to an integrated amount of the photoelectric current.

4. An image sensitive device as claimed in claim 3, wherein an input diode is provided in the charge-coupled device, and a pulse signal is applied to the input diode to initialize the charge stored under the second gate of the charge-coupled device.

* * * * *